SEMICONDUCTOR PACKAGE AND METHOD OF MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the under 35 USC 119(a) benefit of Korean Patent Application No. 10-2015-0109050, filed on Jul. 31, 2015 with the Korean Intellectual Property Office, the entire disclosure of which is incorporated herein by reference for all purposes.

BACKGROUND

[0002] 1. Field

[0003] The following description relates to a semiconductor package and a method of manufacturing the same.

[0004] 2. Description of Related Art

[0005] Currently, in order to connect a top surface and a bottom surface to each other, or to form connection electrodes toward an outer portion of a package on a circuit board, a method of using a copper pin, or forming a via hole in a encapsulation layer and plating an inner portion of the via hole is mainly used.

[0006] However, in a case in which an interval between the connection electrodes is decreased at a fine pitch, there is a problem that both aligning and manufacturing the copper pin are difficult. The method of forming a via hole in an encapsulation layer and plating an inner portion of the via hole is also problematic in that a processing yield is decreased as a via hole is decreased at the fine pitch because a ratio of a diameter of the via hole to an axial length of the via hole is predetermined.

[0007] Further, since it is difficult to consistently form a constant axial length by the method of using a copper pin or plating an inner portion of a via hole, a structural change for forming the connection electrodes is desired.

SUMMARY

[0008] This Summary is provided to introduce a selection of concepts in a simplified form that are further described below in the Detailed Description. This Summary is not intended to identify key features or essential features of the claimed subject matter, nor is it intended to be used as an aid in determining the scope of the claimed subject matter.

[0009] In one general aspect, a semiconductor package includes a first substrate, a pattern layer disposed on the first substrate, a first chip member disposed on a surface of the first substrate, lead frames mounted on the first substrate surrounding the first chip member, and a first encapsulation layer disposed on the first substrate, encapsulating the first chip member and the lead frame, wherein upper end portions of the lead frame and the first encapsulation layer are removed, and lead frame columns are exposed through the first encapsulation layer.

[0010] A plurality of lead frames may be provided along four lateral sides of the first chip member.

[0011] The semiconductor package my further include a second substrate disposed on the first encapsulation layer, a second chip member disposed on the second substrate, and a second encapsulation layer, encapsulating the second substrate and the second chip member. The first substrate and the second substrate may be electrically connected to each other by a plurality of lead frame columns provided along four sides of the first chip member.

[0012] The semiconductor package may further include a second chip member disposed on another surface of the first substrate, opposite to the surface of the first substrate, and a second encapsulation layer, encapsulating the second chip member.

[0013] An upper end portion or a lower end portion, or both end portions, of the lead frame columns may include a bent part.

[0014] The semiconductor package may further include a solder part disposed on a top surface of the lead frame.

[0015] The semiconductor package may further include mounting electrodes disposed on the surface of the first substrate and another surface of the first substrate. The pattern layer may electrically connect to the mounting electrode on the surface of the first substrate to the mounting electrode disposed on the other surface of the first substrate.

[0016] In another general aspect, a method of manufacturing a semiconductor package includes preparing a first substrate, disposing a first chip member on a surface of the first substrate, disposing a lead frame on the surface of the first substrate along a side of the first chip member, disposing a first encapsulation layer onto the surface of the first substrate, wherein the first encapsulating layer encapsulates the first chip member and the lead frame, and removing upper end portions of the first encapsulation layer and the lead frame.

[0017] A plurality of lead frames may be connected to each other by a support. The support may be removed together with the upper end portion of the lead frame.

[0018] Upper end portions of the first encapsulation layer and the lead frame may be removed by polishing, grinding, or cutting.

[0019] An upper end portion, or a lower end portion, or both end portions of the lead frame may include a bent part.

[0020] After the removing of the upper end portions of the first encapsulation layer and the lead frame, the method may further include disposing a second substrate on the first encapsulation layer and the lead frame, disposing a second chip member on the second substrate, and disposing a second encapsulation layer, encapsulating the second chip member.

[0021] After the removing of the upper end portions of the first encapsulation layer and the lead frame, the method may further include disposing one or more second chip members onto another surface of the first substrate, and disposing a second encapsulation layer, encapsulating the second chip members.

[0022] The lead frame may be provided to form a plurality of columns adjacent to each lateral side of the first chip member.

[0023] After the removing of the upper end portions of the first encapsulation layer and the lead frame, the method may further include disposing a solder part on the lead frame.

[0024] The method may further include disposing mounting electrodes on the surface of the first substrate and another surface of the first substrate.

[0025] Other features and aspects will be apparent from the following detailed description, the drawings, and the claims.

BRIEF DESCRIPTION OF DRAWINGS

[0026] FIG. **1** is a cross-sectional view illustrating a semiconductor package according to an embodiment;